1.7 Digital Signaling

One important application of transmission line theory is modeling connections carrying digital signals between logic elements. Two of the main issues that must be dealt with are terminations to reduce reflections and cross-talk between closely spaced lines.

1.7.1 Microstrip

One important type of transmission line that is used for both analog and digital systems is the microstrip, which consists of a conductive strip separated from a ground plane by a dielectric layer (Fig. 1.31). An example is a printed circuit board trace with a ground plane on the bottom of the board.

Figure 1.31: (a) Microstrip transmission line. (b) Dielectric and air replaced by an effective medium with relative permittivity $\varepsilon_r'$.

The microstrip produces electric and magnetic fields in both the dielectric and the air above the dielectric. To a good approximation, the dielectric and air can be replaced by an effective medium everywhere above the ground plane with relative permittivity

$$
\varepsilon_r' = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \sqrt{1 + \frac{10h}{w}}
$$

(1.128)

The inductance per unit length of a microstrip line can be approximated by

$$
L \approx \left\{ \begin{array}{ll}
\frac{60}{c} \ln \left( \frac{8h}{w} + \frac{w}{4h} \right) & \frac{w}{\pi} \leq 1 \\
\frac{12\pi}{c} \left[ \frac{w}{\pi} + 1.393 + 0.667 \ln \left( \frac{w}{\pi} + 1.444 \right) \right]^{-1} & \frac{w}{\pi} \geq 1
\end{array} \right.
$$

(1.129)

The capacitance per unit length is

$$
C \approx \left\{ \begin{array}{ll}
\frac{\varepsilon_r'}{60c\ln \left( \frac{8h}{w} + \frac{w}{4h} \right)} & \frac{w}{\pi} \leq 1 \\
\frac{\varepsilon_r'c}{120\pi c} \left[ \frac{w}{\pi} + 1.393 + 0.667 \ln \left( \frac{w}{\pi} + 1.444 \right) \right]^{-1} & \frac{w}{\pi} \geq 1
\end{array} \right.
$$

(1.130)

These formulas allow microstrip transmission lines to be designed for a given characteristic impedance.

1.8 Printed Circuit Board (PCB) Termination

Consider a connection between two digital logic elements, as shown in Fig. 1.32. This can be modeled as a microstrip transmission line. There are several ways to terminate the system to minimize undesirable reflections on the transmission line.
**No termination.** The FET at the receiver end appears as a high impedance load, which is essentially an open circuit. The load reflection coefficient is \( \Gamma_L \simeq 1 \). For a driver impedance of 10 \( \Omega \) and pulse amplitude 5 V, the initial forward step amplitude is

\[
v_1^+ = \frac{50}{10 + 50} \times 5 \text{ V} = \frac{25}{6} \text{ V} \simeq 4.167 \text{ V}
\]

This wave propagates until it reaches the receiver, at which time it reflects and a reverse pulse propagates towards the driver. The source reflection coefficient is

\[
\Gamma_s = \frac{10 - 50}{10 + 50} = -\frac{2}{3}
\]

Repeated reflections lead to the voltage signal at the receiver end shown in Fig. 1.33.

The change in the voltage decreases by \( \Gamma_L \Gamma_s = -2/3 \) at each bounce. In order for the voltage at the receiver to settle to within 10%, we must have

\[
|\Gamma_L \Gamma_s|^N \leq 0.1
\]

which first occurs when \( N = 6 \). The time required for the voltage to settle to this level is

\[
t_s = 2NT
\]

If the pulse is repeated with a frequency \( f \), we would like to have the voltage settle by at least the middle of the pulse, so that the next pulse is not disturbed too strongly by reflections still occurring from the previous pulse. This means that we must have

\[
t_s \leq \frac{1}{4f}
\]
Substituting the definition of phase velocity and using $N = 6$, for the given example we find that $f < u/(48L)$.

If the line is very short, then the delay time $T$ is small, and so the settling time $t_s$ is also small. In this case, termination may be unnecessary. A rule of thumb is that if the pulse rise time is greater than $6T$, termination is not needed. For example, a trace 6.6” long on standard FR4 PC board has a delay of $T = 1 \text{ ns}$. The pulse rise or fall time must be greater than 6 ns in order to neglect termination.

For a longer line or higher pulse repetition rates, reflections may be intolerable. For $L = 10 \text{ cm}$ and $u = 2 \times 10^8 \text{ m/s}$, we find for the given example that $f < 42 \text{ MHz}$. Alternately, the length of the line must be less than about $0.1 \lambda$. For a digital system, this is a very low operating frequency. To do better, we need to add some kind of termination to the line to reduce the reflections.

**Load termination.** Another way to terminate the connection is to add a matching resistor of value equal to $Z_o$ in parallel with the receiver transistor (Fig. 1.34). This eliminates all reflections. But the power dissipated at the load is

$$P = \frac{V^2}{R} \simeq 4.166^2 \frac{50}{50} \simeq 0.35 \text{ W}$$

For a system with many connections, the total dissipated power would be intolerably large. Moreover, this is more power than can be supplied by a typical driver circuit.

![Figure 1.34: Matching resistor at the load.](image)

**Source termination.** Another termination scheme with less power consumption is to add a resistor at the driver end which increases the effective source impedance to $Z_o$ (Fig. 1.35). The initial forward wave has amplitude $v_1^+ = 2.5 \text{ V}$, and the reflection from the receiver is $v_1^- = 2.5 \text{ V}$. But the reflection coefficient
looking into the driver and source termination is zero, so there is only one bounce, and the settling time is faster than in the case of no termination. Because the receiver still appears as a high impedance load, little current flows and the power dissipated is small. Some potential problems with this approach are that the driver impedance may be different depending on whether it is sourcing or sinking current; multiple loads do not see a “high” voltage at the same time; and there is still some power dissipated due to the source resistance.

Thevenin termination. Another approach is to use a pullup resistor at the receiver (Fig. 1.36). When the driver switches high and a forward wave travels to the load end, there is no reflection, since the termination has value $Z_0$. But in this case the voltage across the resistor is small and not very much current flows through it. The current associated with the reflected wave is almost equal and opposite to the incident current. When the driver goes low, the incident current turns off, so there is a net current flow towards the driver. This setup has the advantage that the driver does not have to supply very much current and only has to sink current when the pulse turns off.

Diode clamp termination. If the diode turn-on voltage is $v_d$, and the incident voltage is $v_i^+$, when the incident pulse arrives at the load, the upper diode in Fig. 1.37 will turn on. The voltage at the load will be clamped at $v_{cc} + v_d$, so the amplitude of the reflected wave is only $v_{cc} + v_d - v_i^-$. For the given example, with $v_d = 0.7 \text{V}$, $v_i^- = 1.53 \text{V}$, which is smaller than the reflection in the case of no termination.

When further reflected forward pulses arrive at the diode, as long as the total current through the diode is positive, the load appears to be a short, since the total voltage at the diode is clamped and new pulses cannot change the load voltage. At some point, the total current through the diode drops to zero and the diode shuts off, and the reflected wave must be determined by requiring the total current (the sum of all forward and
reverse currents) through the diode to be zero. After that, the diode remains off, and the load appears to be an open circuit.

(Time $t = 3T$) For the example circuit, the second forward wave has amplitude $v_2^+ = \Gamma v_1^- \approx -1.022$ V. Since the voltage is clamped to 5.7 V, the reflection cannot change the voltage, so $v_2^- = -v_2^+$. To check and make sure the diode is still on, we need to look at the current through the diode, which at the time of the second reflection is $(v_1^+ - v_1^- + v_2^+ - v_2^-)/Z_o \approx 0.59/Z_o$. Since this is positive, the diode is still on.

(Time $t = 5T$) At the time of the third reflection from the load, the current would go negative if we considered the diode to still be on. So, the diode turns off, and the current through the diode is $(v_1^+ - v_1^- + v_2^+ - v_2^- + v_3^+ - v_3^-)/Z_o$ must be zero. Solving for $v_3^-$ gives a value of $-0.0926$. After this time, the pulse bounces between the source and open load. In the steady state, no current flows, and the load voltage approaches 5 V.

Figure 1.38: (a) Bounce diagram and load voltage plot (b) for diode termination.

The bottom diode will never let the voltage at the load become smaller then $-v_d$. The diodes also protect the other circuit elements from damage due to static discharge.